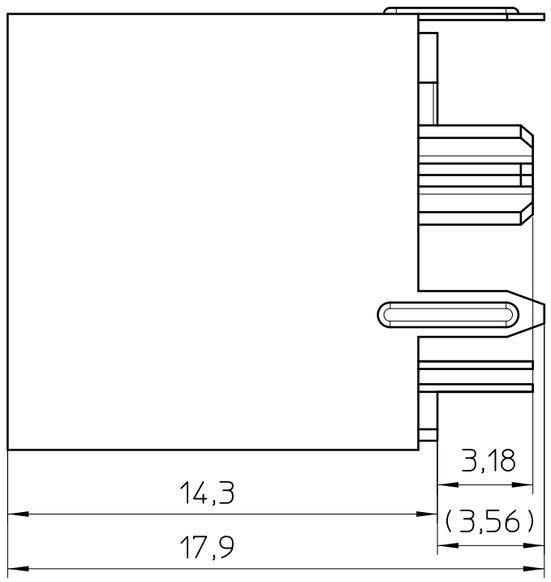
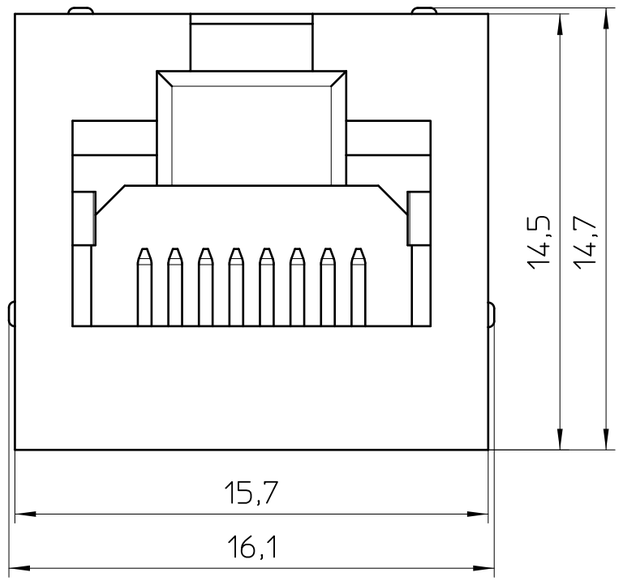
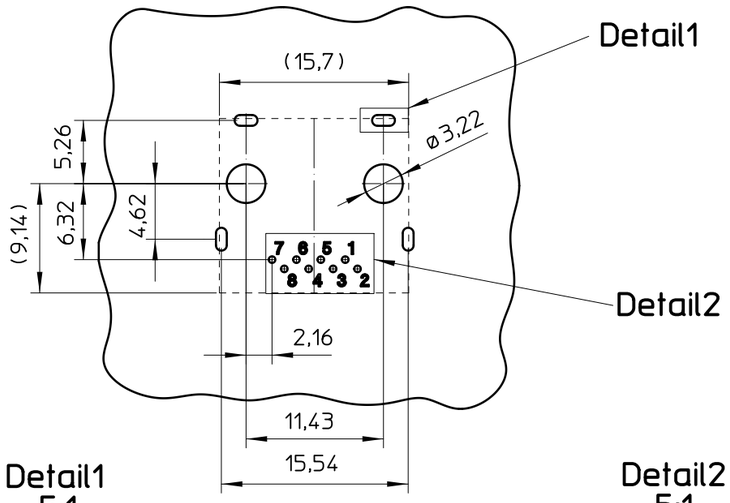
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Tolerance specifications do not include clearances inherent in the design.

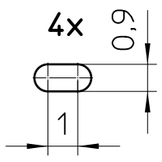




PCB drill hole dimensions
(seen from component side)

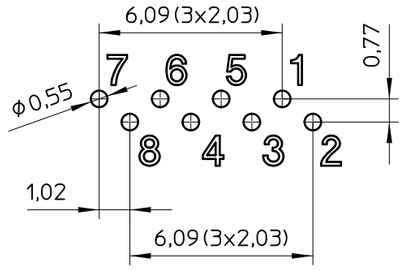


Detail1
5:1

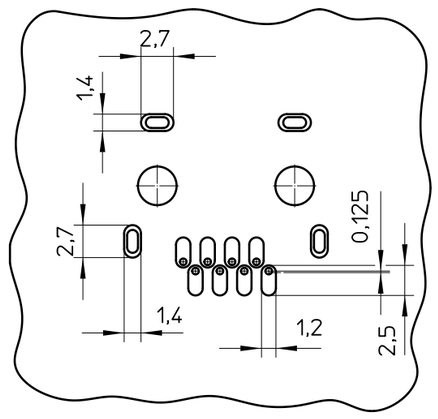


Detail2
5:1

Signal PIN Number Detail



PCB recommended layout for THR and solder wave
copper layer and solder paste mask (150 µm)



DIN A3	document-No. / RI: 01230419 / 04	date: 08.04.2022	scale: 5:1	- Simplified representation - Document excluded from change process - Linear dimensions [mm] - EN ISO 291 23/50
PHOENIX CONTACT	document-type: TECDOC 2D_Productfamily			
page 1 of 1	description: CUC-IND-J1ST-S/R4LS			

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